

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: **Toshio TAKAYAMA, et al.**

Serial Number: **Not Yet Assigned**

Filed: **December 16, 2003**

For.: **SEMICONDUCTOR DEVICE HAVING A MULTILAYER INTERCONNECTION
STRUCTURE AND FABRICATION PROCESS THEREOF**

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

December 16, 2003

Sir:

In compliance with 37 CFR 1.56, Applicants call to the attention of the Patent and Trademark

Office the references listed on the attached PTO-1449.


A copy of each of the references is enclosed herewith.

In the event there are any fees due in connection with the filing of this paper, please charge

Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: PTO-1449; References (3)

INFORMATION DISCLOSURE STATEMENT PTO-1449	Atty. Docket No. 031325	Serial No. New Application
	Applicant(s): Toshio TAKAYAMA, et al.	
	Filing Date: December 16, 2003	Group Art Unit: Not Yet Assigned

U.S. PATENT DOCUMENTS

Examiner Initial	Document No.	Name	Date	Class	Subclass	Filing Date (If appropriate)
_____	AA					
_____	AB					
_____	AC					
_____	AD					

FOREIGN PATENT DOCUMENTS

Document No.	Date	Country	Translation (Yes or No)
_____ AE 2001-93976	04/06/01	Japan	Yes-Abstract
_____ AF 11-8753	01/12/99	Japan	Yes-Abstract
_____ AG 7-94610	04/07/95	Japan	Yes-Abstract
_____ AH			
_____ AI			

OTHER DOCUMENTS

_____	AJ			
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<table border="1" style="width: 100%;"> <tr> <td>Examiner</td> <td>Date Considered</td> </tr> </table>			Examiner	Date Considered
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